

AMENDMENTS TO THE CLAIMS:

Kindly amend claims 1-8 and 12, and add new claims 14-15.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (currently amended): A method of fabricating a wired board with bump electrodes, comprising the steps of:

providing a template formed of a high-concentration impurity semiconductor base;

forming a resist having an opening on ~~[[a]]~~ said high-concentration impurity semiconductor base;

forming a conductive layer in said opening in said resist; and

forming a bump electrode on said wired board by aligning an electrode pad formed on said wired board with said conductive layer and then transferring said conductive layer from said template to said electrode pad.

Claim 2 (currently amended): The fabrication method according to claim 1, wherein said high-concentration impurity semiconductor base has a pit formed at a position where said conductive layer ~~should be~~ is formed.

Claim 3 (currently amended): The fabrication method according to claim 1, wherein the impurity of said high-concentration impurity semiconductor base is ~~[[one]]~~ a material selected from the group consisting of B, P, As, Sb and Pt.

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Claim 4 (currently amended): The fabrication method according to claim 1, wherein said conductive layer is formed of [[one]] a material selected from the group consisting of Au, Cu, Ni, Pt, Pd, Ag, Sn and Pb, and an alloy thereof.

Claim 5 (currently amended): The fabrication method according to claim 1, wherein said conductive layer is formed of paste containing [[one]] a material selected from the group consisting of Au, Cu, Ni, Pt, Pd, Ag, Sn and Pb, and an alloy thereof.

Claim 6 (currently amended): The fabrication method according to claim 1, wherein said conductive layer is formed by [[one]] a method selected from the group consisting of electrolytic plating, electroless plating, sputtering, vapor deposition and printing.

Claim 7 (currently amended): The fabrication method according to claim 1, wherein at least the region on said high-concentration impurity semiconductor base where said conductive layer is formed [[are]] is roughed.

Claim 8 (currently amended): The fabrication method according to claim 1, wherein at least the region on said high-concentration impurity semiconductor base where said conductive layer is formed [[are]] is subjected to strike plating.

Claim 9 (original): The fabrication method according to claim 2, wherein a size of said opening in said resist is smaller than a size of opening of said pit.

Claim 10 (original): The fabrication method according to claim 2, wherein a size of said opening in said resist is larger than a size of opening of said pit.

Claim 11 (original): The fabrication method according to claim 2, wherein the position of said

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opening in said resist is shifted from the position of opening of said pit.

Claim 12 (currently amended): The fabrication method according to claim 2, wherein said pit ~~[[takes]]~~ has a shape selected from the group consisting of a pointed shape, a pentahedron shape, a pyramid shape and a hemispherical shape.

Claim 13 (original): The fabrication method according to claim 2, wherein a depth of said pits is equal to or greater than $\frac{1}{4}$ of a thickness of said resist.

Claim 14 (new): The fabrication method of claim 1, wherein high-concentration impurity semiconductor base has an impurity concentration of $1 \times 10^{17} \text{ cm}^{-3}$ or higher.

Claim 15 (new): The fabrication method of claim 1, wherein the high-concentration impurity semiconductor base has an impurity concentration in the range of $1 \times 10^{15} \text{ cm}^{-3}$ to $1 \times 10^{22} \text{ cm}^{-3}$.

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